

**WHAT IS CLAIMED IS:**

1. A method of driving a liquid crystal display device, wherein the liquid crystal display device includes a gate line; a data line crossing the gate line; a dummy gate line adjacent the gate line; a thin film transistor connected to the gate and data lines; a first capacitor receiving signals from the thin film transistor; and a storage capacitor connected to the first capacitor, the method comprising applying a dummy gate signal to the dummy gate line, wherein the dummy gate signal has a substantially same waveform as a gate signal applied to the gate line.
2. The method of claim 1, wherein the gate signal is a pulse signal having a high period of one horizontal line period.
3. The method of claim 1, wherein the dummy gate signal is a pulse signal having a high period of one horizontal line period.
4. The method of claim 3, wherein the high period of the dummy gate signal precedes the high period of the gate signal by one horizontal line period.
5. A driving circuit of a liquid crystal display device, wherein the liquid crystal display device includes a gate line; a data line crossing the gate line; a dummy gate line adjacent the gate line; a thin film transistor connected to the gate and data lines; a first capacitor receiving signals from the thin film transistor; and a storage capacitor connected to the first capacitor, the driving circuit comprising:
- a gate driver producing a gate signal, the gate signal being applied to the gate line;
  - a data driver producing a data signal, the data signal being applied to the data line;
- and
- a dummy gate driver producing a dummy gate signal of a substantially same waveform as the gate signal, the dummy gate signal being applied to the dummy gate line.
6. The driving circuit of claim 5, wherein the dummy gate driver includes first and second

flip-flops and a level shifter.

7. The driving circuit of claim 6, wherein a vertical synchronizing signal and a data enable signal are input to the dummy gate driver.

8. A method of driving a display comprising generating a plurality of data signals corresponding to gate signals, a first one of the data signal corresponding to a first one of the gate signals being an invalid data.

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